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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,494	02/13/2001	Stephen L. Buchwalter	YOR920000745US1(14029)	9921

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EXAMINER

NGUYEN, KHIEM D

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/782,494

Applicant(s)

BUCHWALTER ET AL.

Examiner

Khiem D Nguyen

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) 23-32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-22 in Paper No. 3 is acknowledged.

Specification

2. Claim 1 is objected to because of the following informalities: In claim 1, line 2, change "undefill layer" to "underfill layer". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilleo et al. (U.S. Patent 6,228,678).

Gilleo teaches a method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of (see col. 1, line 61 to col. 9, line 33 and FIGS. 1-5):

(a) forming a first polymeric material 14 composed of epoxies has a thickness of from about 25 to about 100 microns by a deposition process such as spin coating on a surface of a semiconductor wafer 12 having interconnect pads 15 disposed thereon and said wafer has one or more devices present therein and the first polymeric material further includes an inorganic filler comprises of silica wherein said inorganic filler is present in said first polymeric material in an amount of from about 10-80 % by weight;

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(b) patterning said first polymeric material to provide openings 16 that expose said interconnect pads by etching;

(c) forming conductive bump material 18 such as solder bumps in said openings by a plating method;

(d) forming a second polymeric material 20 composed of flux material over said first polymeric material and said conductive bump material wherein the second polymeric material has a thickness that is thinner than the first polymeric material;

(e) dicing said semiconductor wafer into individual chips; and

(f) bonding at least one of said individual chips to an external substrate such as circuit board or chip carrier, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate;

Gilleo teaches the first polymeric material is formed by spin coating but fails to teach that the second polymeric material is formed by spin coating as recited in present claim 14.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply Gilleo's teaching to form the second polymeric material by spin coating because doing so can provide a smooth and level coating. See col. 5, lines 11-15.

Gilleo teaches that the first polymeric material is a thermoplastic but fails to teach the second polymeric material is a thermoplastic as recited in present claim 16.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to apply Gilleo's teaching to form the second polymeric material such that the second polymeric material is a thermoplastic because doing so can eliminate the problems associated with thermoset underfills. See col. 7, lines 29-32.

Gilleo fails to teach the thickness of the second polymeric material as recited in present claim 18.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal thickness for the second polymeric material through routine experimentation and optimization to obtain optimal or desired device performance because the thickness of the second polymeric material is result-effective variables and there is no evidence indicating that the thickness of the second polymeric material is critical and it has been held that it is not inventive to discover the optimum or workable thickness of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Gilleo fails to teach the ranges for the temperature and time duration of the bonding step as recited in present claim 19.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for the temperature and time duration of the bonding step through routine experimentation and optimization to obtain optimal or desired device performance because the ranges for the temperature and time duration of the bonding step are result-effective variables and there is no evidence indicating that the ranges for the temperature and time duration of the

bonding step are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilleo et al. (U.S. Patent 6,228,678).

Gilleo teaches a method of forming a microelectronic interconnect structure containing a bilayer underfill layer comprising the steps of (see col. 1, line 61 to col. 9, line 33 and FIGS. 1-5):

(a) forming a first polymeric material 14 composed of epoxies on a surface of a semiconductor wafer 12 having conductive bump material 18 disposed on portions thereof;

(b) removing a portion of said first polymeric material so as to expose top surfaces of said conductive bump material by etching;

(c) forming a second polymeric material 20 composed of flux material on said first polymeric material and said exposed top surfaces of said conductive bump material;

(d) dicing said semiconductor wafer into individual chips; and

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(f) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate;

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
June 14, 2002

L. Ph
LONG PHAM
PRIMARY EXAMINER